DESIGN AND SIMULATION OF A TYPICAL HIGH PERFORMANCE AHB RECONFIGURABLE MASTER FOR ONCHIP BUS ARCHITECTURE USING VERILOG HDL

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ABSTRACT

Resolution is a big issue in system on chip while dealing with number of masters trying to sense a single data bus. This paper presents the Design and Simulation of a typical High Performance AHB Reconfigurable Master for Onchip Bus Architecture using verilog HDL. In this methodology I here used wrap logic to generate data at specific time by several bus masters. The key point in this paper is wrap logic. The FSM for AHB master has been generated and simulated on modelsim HDL tool. The scheme involves several AMBA features of pipelined operation, multiple bus masters, burst transfers, split transations. The purpose of this paper is to propose a scheme to implement reconfigurable architectures so that it can be interfaced with any IP core as such a system using AMBA busspecification.

Here we proposed generation of AMBA ABH master using wrap logic. The design architecture is written using Verilog HDL using Modelsim tool. The timing diagrams are also generated on this tool. The synthesis of the design is done on Xilinx tool. The mapping, floorplaning, places and routes are also generated on Xilinx tool.

Keywords*-reconfigurable master, split transation,burst transfer,wrap logic, AMBA, AHB, Verilog HDL, Xilinx, FPGA.*

INTRODUCTION TO AMBA

The Advanced Microcontroller Bus Architecture (AMBA) specification defines on chip communication standards for designing high-performance embeddedmicrocontrollers.

Three buses are defined in this specification:

1) the Advanced High Performance Bus(AHB)
2) the Advanced SystemBus(ASB)
3) the Advanced Peripheralbus(APB)

ADVANCED HIGH-PERFORMANCE BUS(AHB)

This bus is used for high-performance, high clock frequency system modules. This bus is acts as the backbone bus. AHB efficiently interconnects processors, on-chip memories and off-chip external memories interfaces with low-power peripherals macrocell functions.

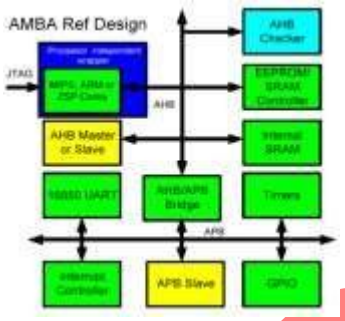

Fig.1 A typical AMBA system

AHB BUS SPECIFICATION

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. AMBA AHB is a new level of bus which sits above the APB and implements the features required for high-performance, high clock frequency system including:

A. bursttransfers
B. splittransitions
C. single cycle bus masterhandover
D. single clock edgeoperation
E. non-tristateimplementation
F. Larger data bus configurations (64/128bits).

AHB BUS MASTER INTERFACE

An AHB bus master has the most complex bus interface is an AMBA system. In this paper I implement this AMBA ABH master using wrap logic. Since there are several master can be used in AMBA specification so the arbiter can choose any one of that at the time of transfer. The interface diagram of ABH bus master shows the main signal groups.

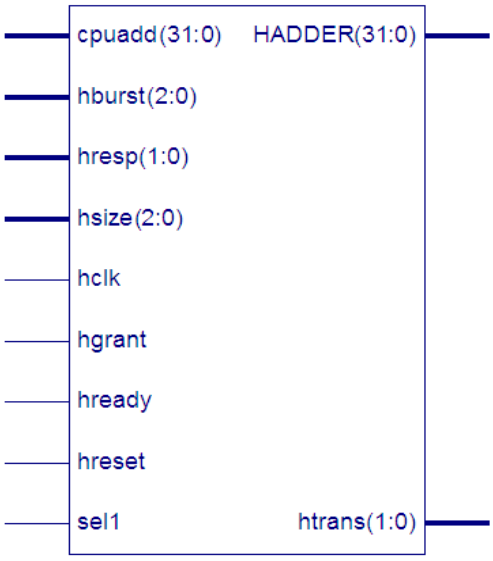

Fig.2 AHB bus master interface

DATA PATH

The ABH Master can be broken into sub systems.The two major components of the system under design are the controller and data path.The data path are further divided into several subsystems. All these subsystems are then controlled by the top module and a FSM module.Some of these data path are as follows-

1. **Control unit block:-**Different inputs from the arbiter like hready, hclk, hreset are using as inputs to this block.this block then generate a datadone signal asoutput.
2. **Early burst generation and termination block:-**There are several circumstances when a burst will not be allowed to complete and therefore it is important that any slave design which makes use of the burst information can take the correct course of action if the burst is terminated early. The slave can determine when a burst has terminated early by monitoring the HTRANS signals and ensuring that after the start of the burst every transfer is labeled as SEQUENTIAL or BUSY. If a NONSEQUENTIAL or IDLE transfer occurs then this indicates that a new burst has started and therefore the previous one must have been terminated. For example, if a master has only completed one beat of a four-beat burst then it must use an undefined-length burst to perform the remainingtransfers.
3. **Burst transfer block:-** A granted bus master starts an AMBA AHB transfer by driving the address and control signals. These signals provide information on the address, direction and width of the transfer, as well as an indication if the transfer forms part of a burst. Two different forms of burst transfers areallowed-
   a) incrementing bursts, which do not wrap at addressbiundaries
   b) wrapping bursts, which wrap at particular addressboundaries**.**
4. Counter(4 bit)
5. Multiplexor(2×1 and8×1)
6. Adder (16bit)

DEVICE UTILIZATION SUMMARY

Selected device: xcv50-6fg256

Number of Slices	124
Number of Slice Flip Flops	66
Number of 4 input LUTs	242
Number of Bonded IOBs	76

Table.1

Total equivalent gate count for design: 2970
Total JTAG countfor IOBs : 3696

RESULTS AND SIMULATION

The design is simulated on modelsim. The advantage of this design is that we have taken care of area consumption hence with less latch and maximum flip-flops have enhanced our area efficiency. FSM coding has been done for controller design. The resulting simulation timing diagram, RTL view and Floorplan results are shown below:-

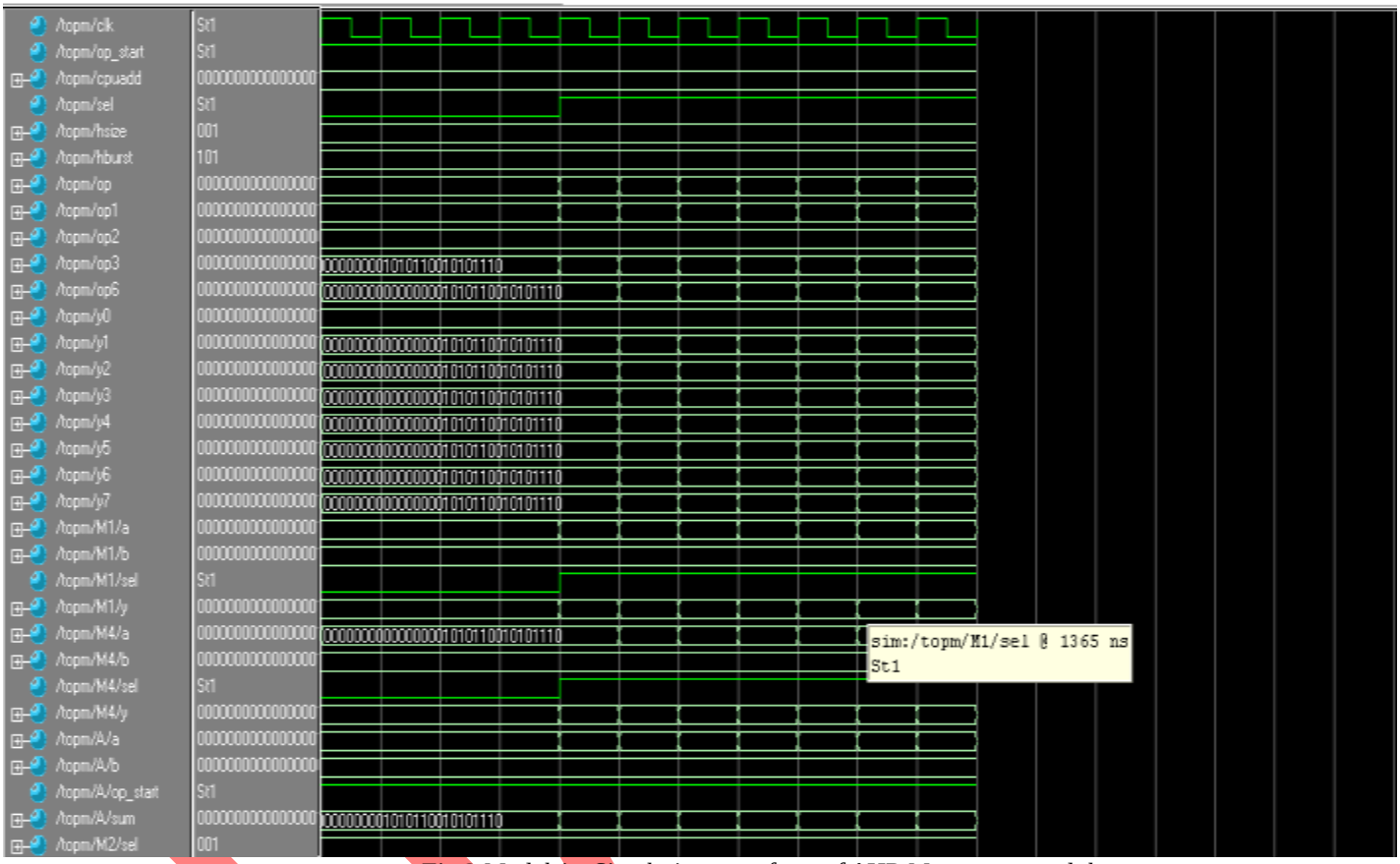

Fig.3 Modelsim Simulation waveform of AHB Master top module

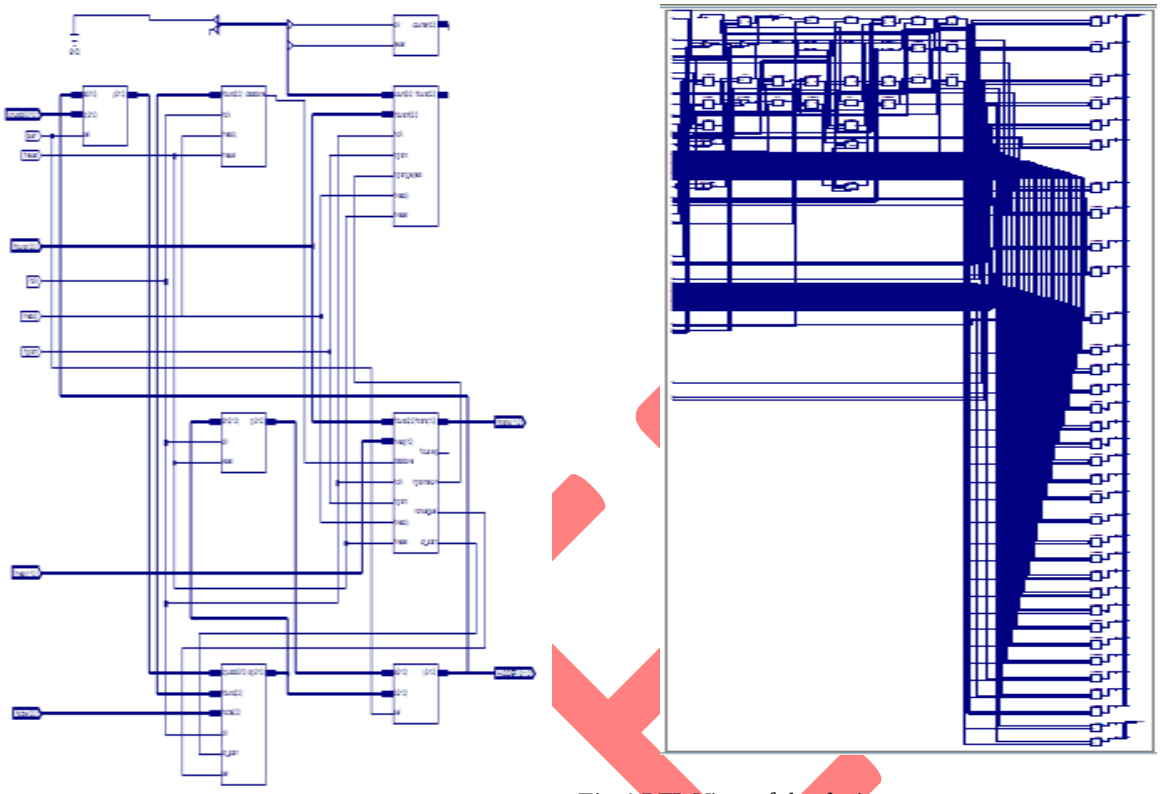

Fig.4 RTL View of the design

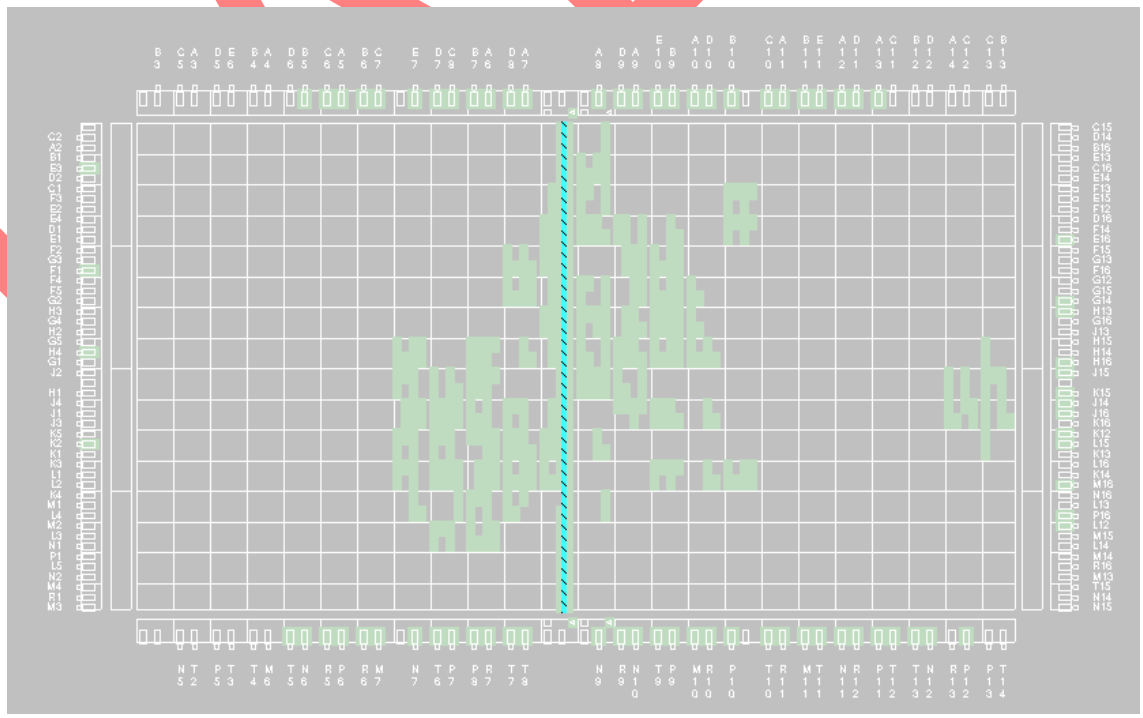

Fig.5 Floorplan of the design

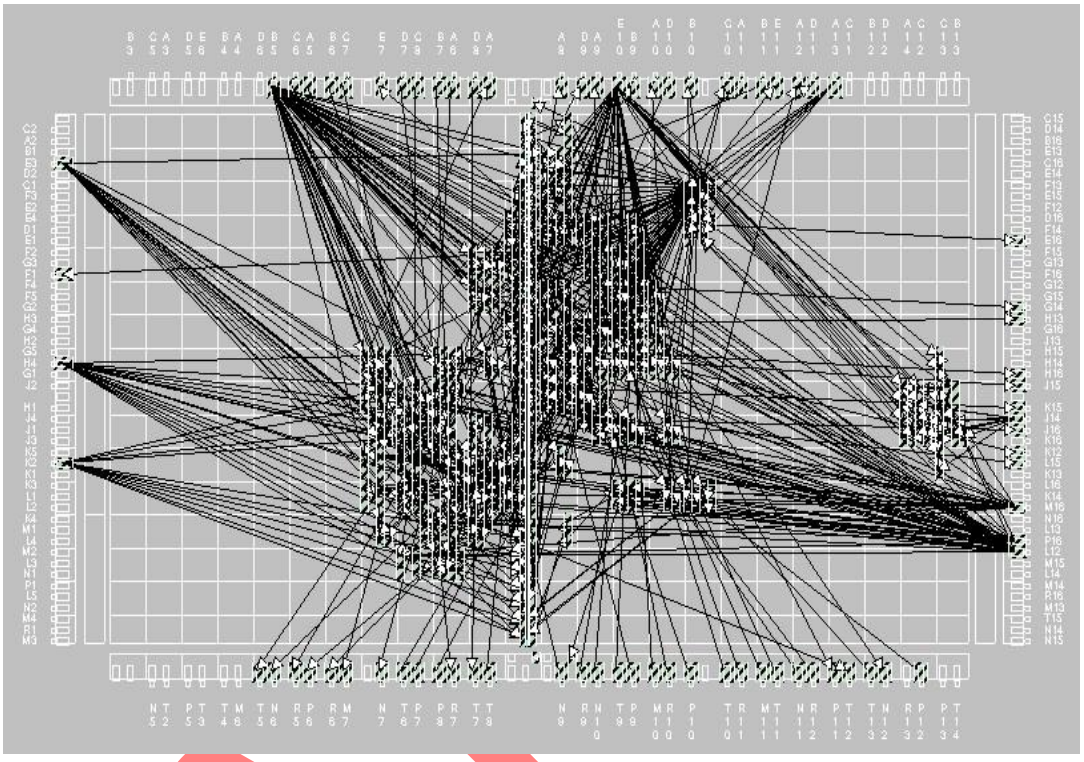

Fig.6 Places and route on the device

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